REMARKS

Claims 1, 3, 14-29 and 31-36 are pending in this application, of which claims 29 has been amended. Claims 2, 4-13 and 30 have been canceled. Claims 17-28 have been withdrawn from consideration. No new claims have been added.

Claims 1-3, 14-16, 29 and 31-36 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite.

In particular, the Examiner is unclear about the following points regarding claims 1 and 14:

1. How does the time difference expander determine the first and second changeover points of the first and second signals?

2. How does the time difference expander expand the time difference between the first and second changeover points?

3. Is there some sort of edge detection device included in the time difference expander (variable delay circuit)?

The Examiner is also unclear regarding the following points with respect to newly-added claims 29 and 36:

1. Is the first clock signal represented by the input clock signal (CLK) or the first signal (A)?

2. If the first clock signal (A) is the first clock signal recited in claims 29 and 36, then how does the first delay circuit receive the first clock signal? (The Examiner understands that the first delay signal receives the input clock signal (or control clock signal CLK.))

In response to these questions, Applicant respectfully submits the following explanation of the claimed invention.

A time difference expander expands a time difference (t) between a rising edge of a first signal A and a falling edge of a second signal B. This expanding process will be explained below with reference to FIG. 15.

In FIG. 15, when the second signal B (= CLK) is at a high level "H", a forward gate array (first gate chain AA) is activated and a reverse gate array (second gate chain BB) is inactivated, common nodes between the forward gate array and the reverse gate array (a group of wirings each connecting the gates of first and second gate chains) transfer a signal from left to right.

In this state, the first signal A (which is supplied to an input IN(AA) of the forward gate array AA) is changed from a low level "L" to a high level "H" and a rising edge of the first signal A (which is called "Event A") is generated; the Event A is transferred from left to right in the forward gate array (AA).

Thereafter, when the second signal B (= CLK) is changed ("transition") from the high level "H" to the low level "L" and falling edge of the second signal B (which is called "Event B") gates after the changeover point (right side gates from the changeover point) of the forward gate array (AA) are inactivated, and gates after the changeover point (left side gates from the changeover point) of the reverse gate array (BB) are activated. Therefore, Event B is transferred from right to left in the reverse gate array (BB) from the changeover point. This signal (Event B) is started by Event A.

In this case, assuming that delay times of all gates included in both of the forward gate array (AA) and the reverse gate array (BB) are the same, a signal having the time difference t between the rising edge of the first signal A and the falling edge of the second signal B in the forward gate array

(AA) passes through the reverse gate array (BB) where the same time difference t is added, and is output from an output terminal OUT of the reverse gate array (BB).

Therefore, the delay circuit shown in FIG. 15 has a function of reproducing the time difference t after "Falling Edge" of the second signal B (= CLK).

With specific regard to question no. 2, an explanation of how the time difference expander expands the time difference between the first and second changeover points (rising edges) is given below.

It should be noted that the time difference expander does not recognize the changeover point, but replaces the time difference t determined between the rising edge of the first signal A and the falling edge of the second signal B with a corresponding number of gate stages, and then the corresponding number of gate stages reproduces the same time difference t.

Thus, the 35 U.S.C. § 112, second paragraph, rejection should be withdrawn.

Claim 29 has been amended to correct a typographical error.

In view of the aforementioned amendments and accompanying remarks, claims 1, 3, 14-29 and 31-36, as amended, are in condition for further examination on the merits.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Petition for Extension of Time
Check in the amount of $120.00

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